TEA2019

CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

- DIRECT DRIVE OF THE EXTERNAL SWITCHING TRANSISTOR
- POSITIVE AND NEGATIVE OUTPUT CURRENTS UP TO 0.5A
- CURRENT LIMITATION
- TRANSFORMER DEMAGNETIZATION AND POWER TRANSISTOR SATURATION SENSING
- FULL OVERLOAD AND SHORT-CIRCUIT PROTECTION
- PROPORTIONAL BASE CURRENT DRIVING
- LOW STANDBY CURRENT BEFORE STARTING (1.6mA)
- SYNCHRONIZATION CAPABILITY WITH INTERNAL PLL
- THERMAL PROTECTION

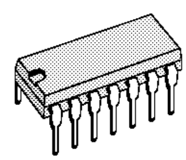
DESCRIPTION

The TEA2019 is an 14-pin DIP low cost integrated circuit designed for the control of switch mode power supplies. It has the same basic functions as the TEA2018A but with synchronization capability by internal PLL. It is particularly suitable for applications where oscillator synchronization is required.

Due to its current mode regulation, the TEA2019 facilitates design of power supplies with following features :

- High stability regulation loop.
- Automatic input voltage feed-forward in discontinuous mode fly-back.
- Automatic pulse-by-pulse current limitation.

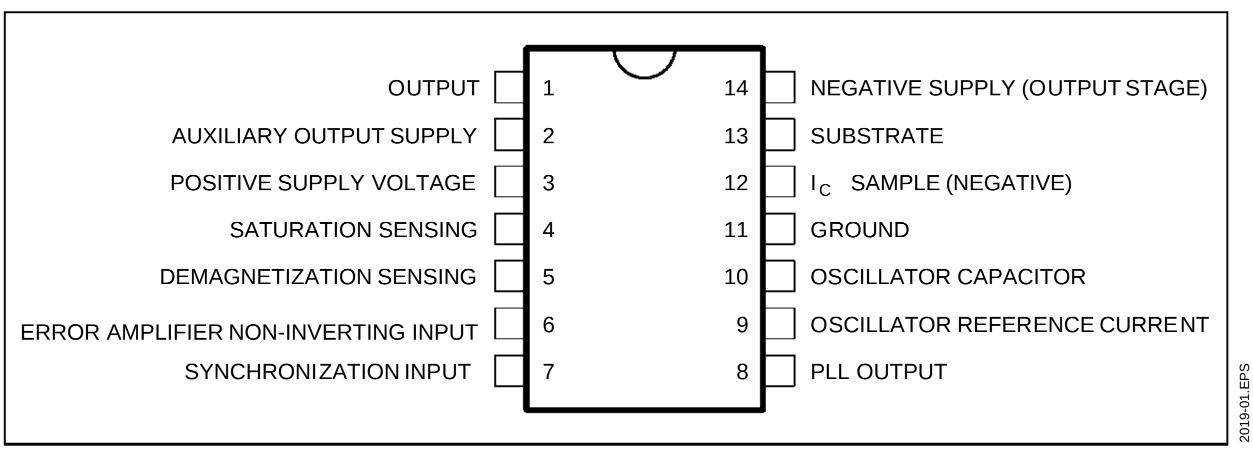
Typical applications : Video Display Units, TV sets, typewriters, micro-computers and industrial applications. For more details, see application note AN406/0591.



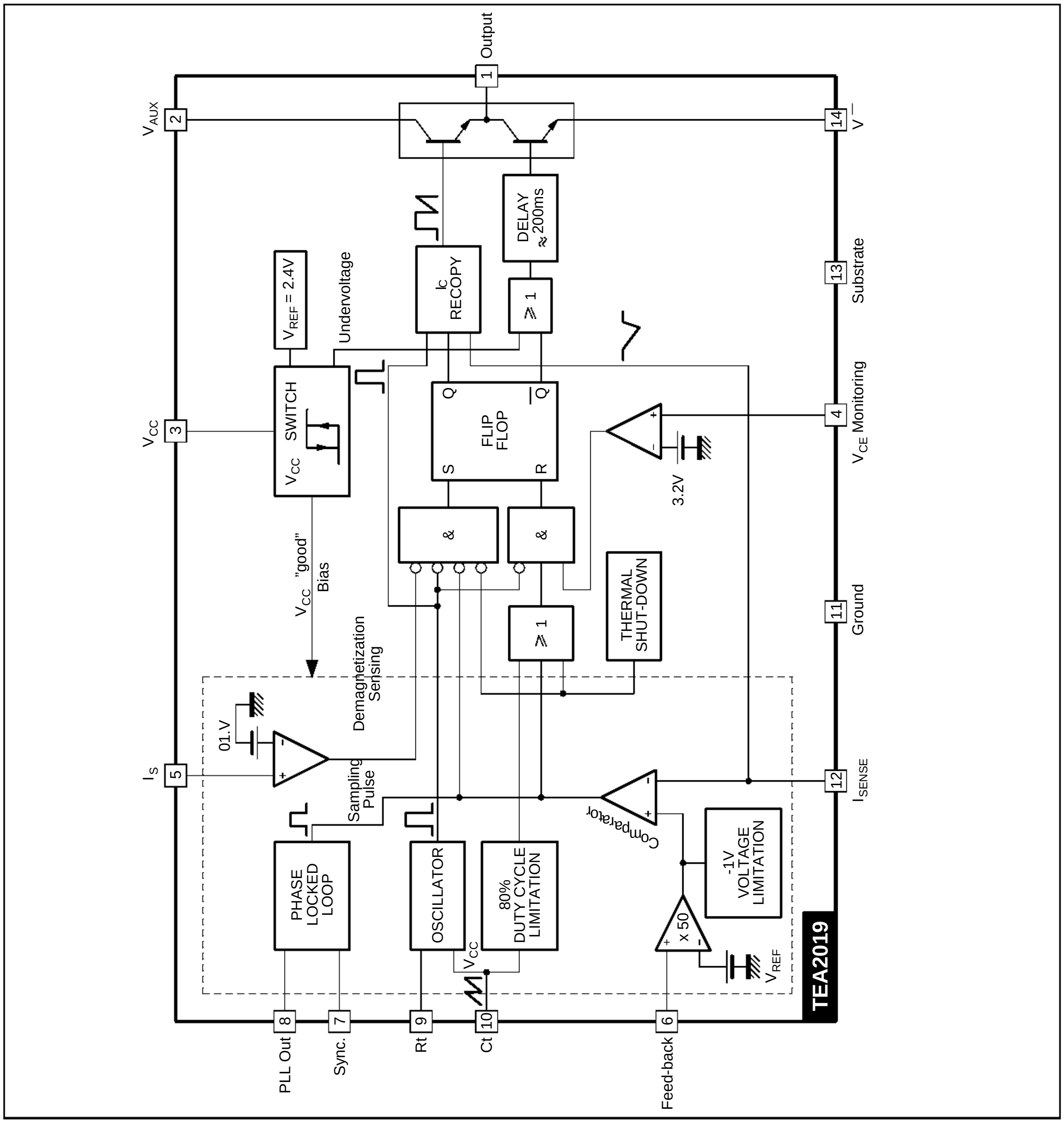
DIP 14
(Plastic package)

ORDER CODE : TEA2019

PIN CONNECTIONS



BLOCK DIAGRAM



2019-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^{+}_{CC}	Positive Supply Voltage	15	V
$V_{(aux)}$	Auxiliary Output Supply Voltage	15	V
V^{-}_{CC}	Negative Supply Voltage	– 5	V
I_O (peak)	Peak Output Current (duty cycle < 5%)	± 1	A
I_I	Input Current Pins 4-5	± 5	mA
T_j	Junction Temperature	150	°C
T_{oper}	Operating Ambient Temperature Range	– 20, + 70	°C
T_{stg}	Storage Temperature Range	– 40, + 150	°C

2019-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

2019-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, potentials referenced to ground (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+_{CC}	Positive Supply Voltage	6.6	8	15	V
V_{CC}	Negative Supply Voltage	–1	–3	–5	V
$V_{CC(start)}$	Minimum positive supply voltage required for starting (V^+_{CC} rising)		6	6.6	V
$V_{CC(stop)}$	Minimum positive voltage below which device stops operating (V^+_{CC} falling)	4.2	4.9	5.6	V
ΔV^+_{CC}	Hysteresis on V^+_{CC} Threshold	0.7	1.1	1.6	V
$I_{CC(sb)}$	Standby Supply Current Before Starting [$V^+_{CC} < V_{CC(start)}$]		1	1.6	mA
$V_{th\ (Ic)}$	Current Limitation Threshold Voltage (pin 12)	–1100	–1000	–880	mV
$R_{(Ic)}$	Collector Current Sensing Input Resistance		1000		Ω
I_S	Demagnetization Sensing Threshold	75	100	125	mV
	Demagnetization Sensing Input Current (pin 5 grounded)		1		µA
τ_{max}	Maximum Duty Cycle	70	80		%
A_V	Error Amplifier Gain		50		
I^+_I	Error Amplifier Input Current (non-inverting input) (pin 6)		2		µA
$V_{(REF)}$	Internal Reference Voltage	2.3	2.4	2.5	V
$\frac{\Delta V_{(REF)}}{\Delta T}$	Reference Voltage Temperature Drift		10^{-4}		V/°C
T_{OSC}	Oscillator Free-running Period (R = 59kΩ, C = 1.5nF)	60	65	70	µs
$\frac{\Delta f_{OSC}}{\Delta T}$	Oscillator Frequency Drift with Temperature (V^+_{CC} = + 8V)		0.05		%/°C
$\frac{\Delta f_{OSC}}{\Delta V_{CC}}$	Oscillator Frequency Drift with V^+_{CC} (+ 8V < V^+_{CC} < + 14V)		0.5		%/V
$t_{on(min)}$	Minimum Conducting Time (C_t = 1nF)		2		µs

2019-03.TBL

SYNCHRONIZATION INPUT (pin 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{7pp}	Peak to Peak Sawtooth Voltage		0.5	2.5	V
$R_{(7)}$	Input Impedance		20		kΩ

2019-04.TBL

PLL CHARACTERISTICS (see Test Circuit)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Frequency Sensitivity		100		Hz/µA
ΔT	Capture Range (T_{OSC} = 64µs Typ.) T_{OSC} - $T_{SYN\ min}$ $T_{SYN\ max}$ - T_{OSC}	5.5 4.5	8 8		µs µs

2019-05.TBL

SATURATION SENSING (pin 4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{(4)}$	Input Threshold		3.2		V
$I_{(4)}$	Input Current (V_4 > 3.2V)	50			µA
	Input Internal Resistance		1		kΩ

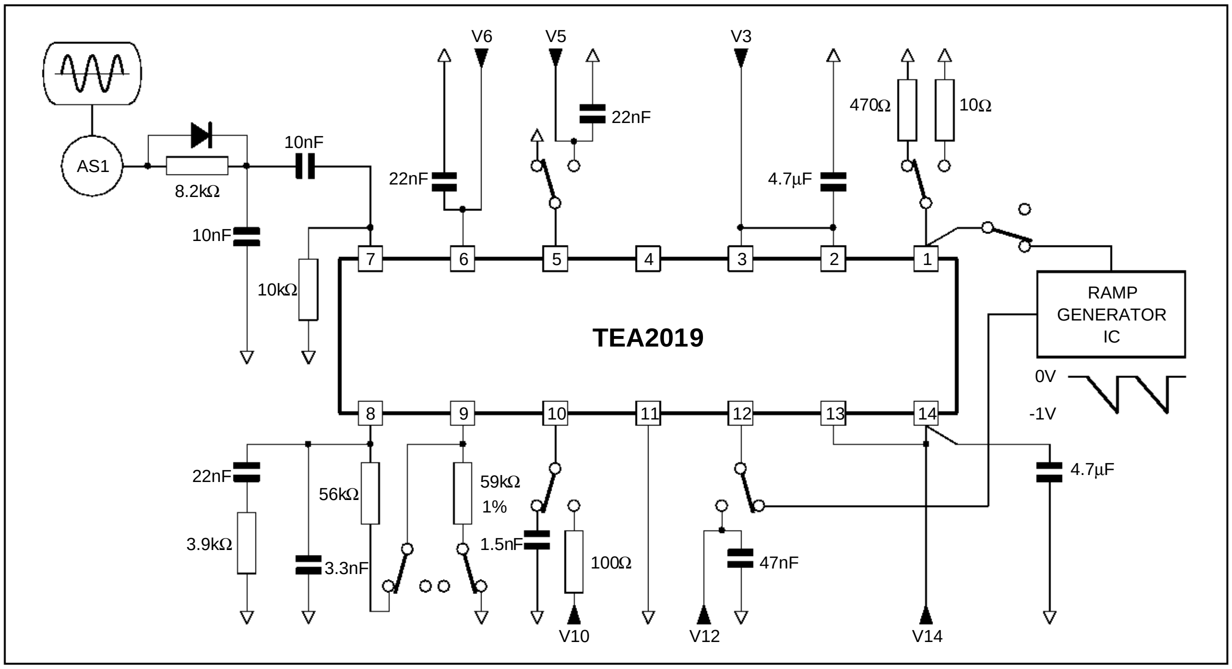
2019-06.TBL

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+_{CC}	Positive Supply Voltage		8		V
V_{CC}	Negative Supply Voltage		3		V
I_O	Output Current			0.5	A
F_{oper}	Operating Frequency		30		kHz

2019-07.TBL

TYPICAL CIRCUIT



2019-03.EPS

GENERAL DESCRIPTION

(see application note AN406/0591)

Operating Principles (Figure 1)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator saw-tooth which acts as clock signal. The period T_{OSC} is given by :

$T_{OSC} \approx 0.69\, C_t\, (R_t + 2000)$

(T_{OSC} in seconds, C_t in Farad, R_t in Ω)

The end of the conduction time is determined by a signal issued from comparing the following signals.

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor.

b) the output of the error amplifier.

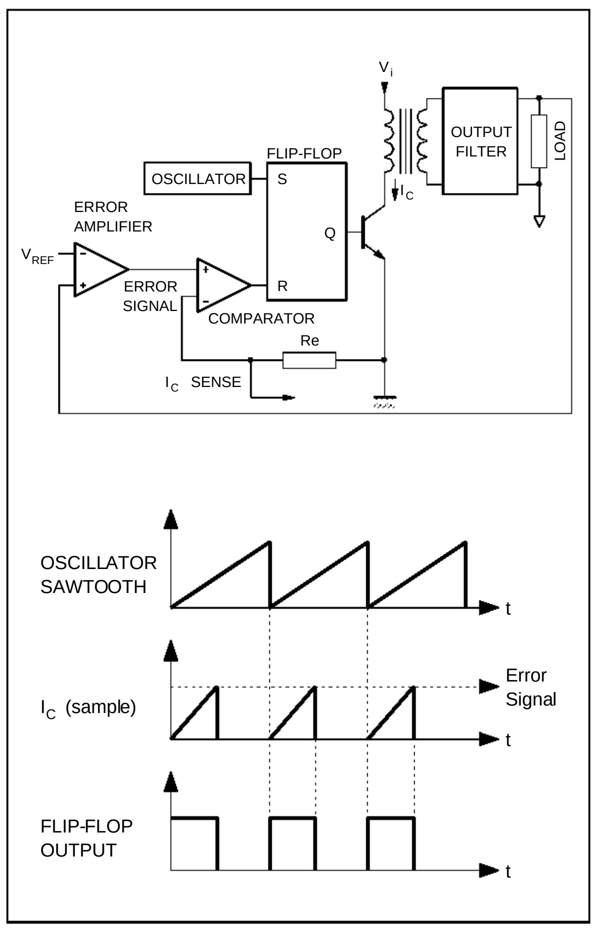
Base Drive

- Fast turn-on
  On each period, a current pulse ensures fast transistor switch-on.
  This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.
- Proportional base drive
  In order to save power, the positive base current after the starting pulse becomes an image of the collector current.

The ratio $\frac{I_C}{I_B}$ is programmed as follows (Figure 2).

$$\frac{I_C}{I_B} = \frac{R_B}{R_E}$$

Figure 1 : Current Mode Control



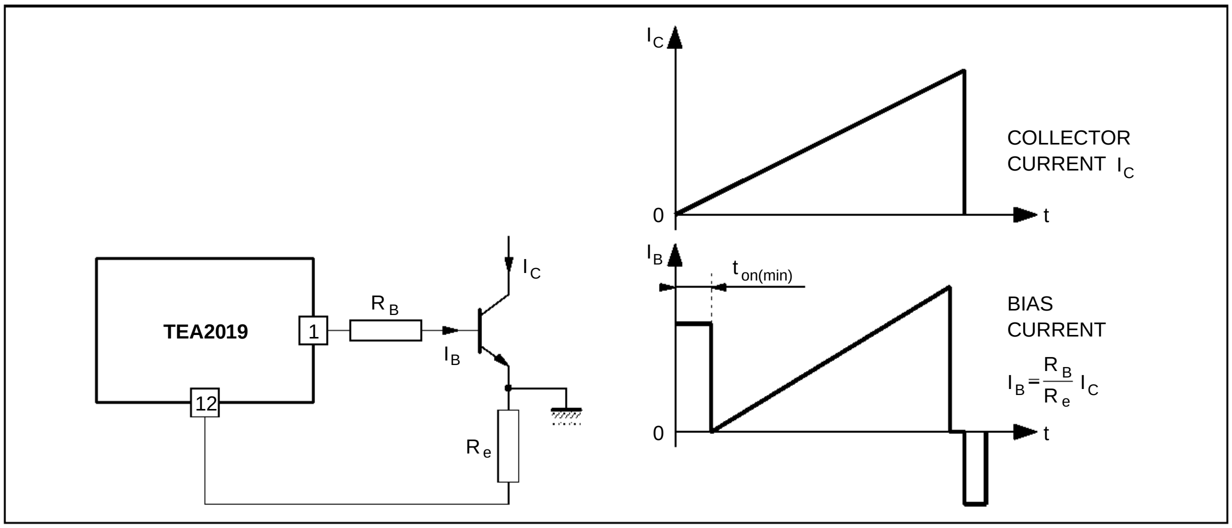
2019-05.EPS / 2019-04.EPS

- Efficient and fast switch-off
When the positive base drive is removed, 1s (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

Safety Functions

- Overload & short-circuit protection
When the voltage applied to pin 12 exceeds the current limitation thershold voltage [$V_{th(Ic)}$], the output flip-flop is reset and the transistor is turned off.
The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin 12 at the maximum allowable collector current.
- Demagnetization sensing
This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized.
When not used, pin 5 must be grounded.
- $t_{on(max)}$
Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70% of the period.
- $t_{on(min)}$
A minimum conducting time is ensured during each period (see Figure 2).
- Supply voltage monitoring
The TEA2019 will stop operating if V_{CC}+ on Pin 3 falls below the threshold level $V_{CC(stop)}$.

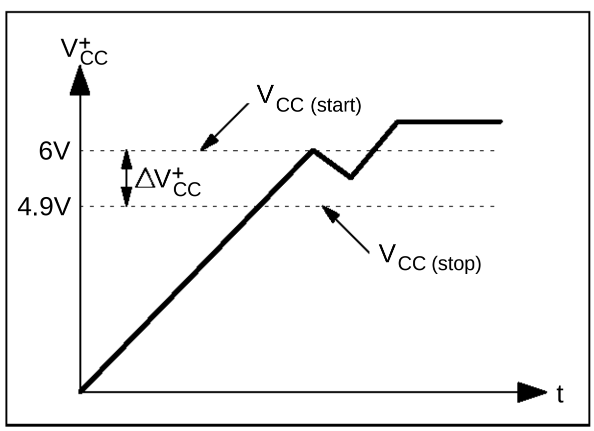
Figure 2



Starting Process (Figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor. This current charges the power supply storage capacitor of the device.
No output pulses are available before the voltage on pin 3 has reached the threshold level [$V_{CC(start)}$, V^{+}_{CC} rising].
During this time the TEA2019 draws only 1mA (typically). When the voltage on pin 3 reaches this threshold base drive pulses appear.
The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1V (typically) (Δ V_{CC}) is implemented to avoid the device from stopping.

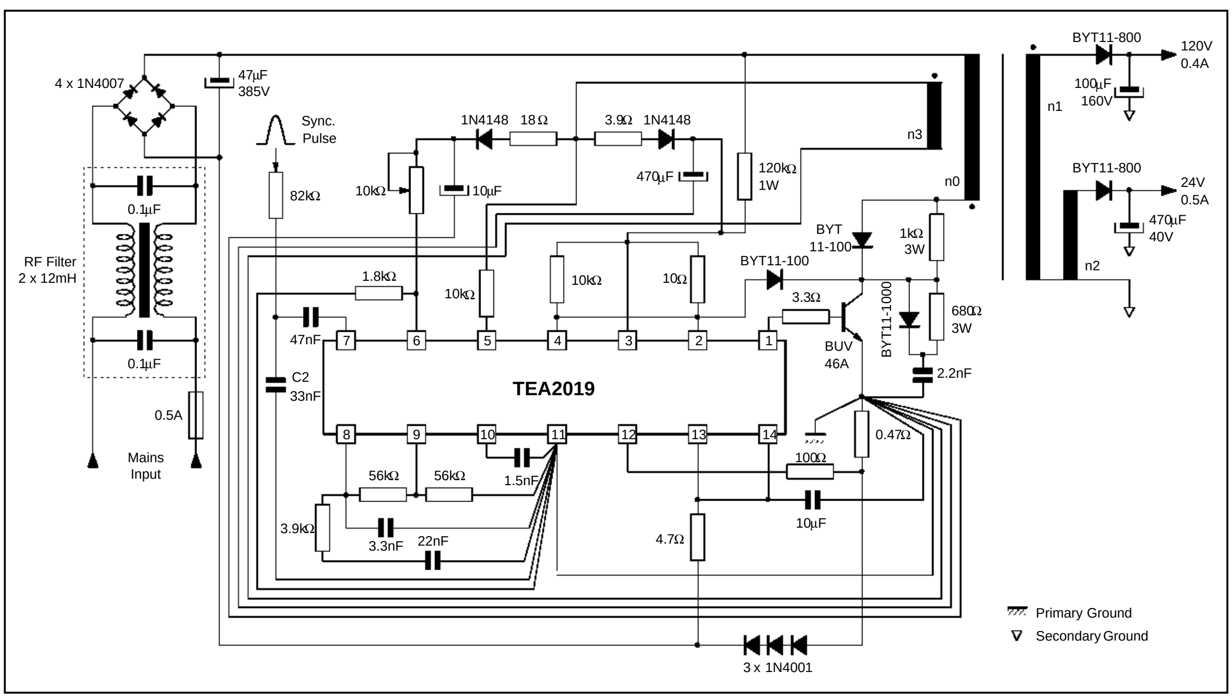
Figure 3 : Normal TEA2019 Start up Sequence



The TEA2019 has some additional capabilities compared to the TEA2018A :

- The oscillator charge current its supplied through an internal current generator, programmed externally - instead of using an external charging resistor. The sawtooth so obtained is linear.
- The oscillator can be synchronized through an internal PLL circuit. This feature provides synchronization between the external sync pulse and the end of the switching transistor current. The sync pulse can be for example the fly-back pulse of a TV horizontal sweep circuit. As indicated in the application diagram, this pulse is applied first to a R.C. network to obtain a low voltage sawtooth and then to pin 7 of the circuit. The PLL output (pin 8) supplies a correction current to pin 9 through an external resistor, so as to maintain the oscillator at the correct frequency (refer to application note AN406/0591 for detailed information).
- In the TEA2019, the power supply of the positive output stage is separated from the main power supply, so that it can be supplied from a lower voltage in order to reduce the I.C. power dissipation.
  For low power applications, the circuit can be normally supplied by connecting pins 2 and 3 together.
- In order to protect the substrate (pin 13) from the parasitic voltage peaks produced by negative output current peaks at pin 14, the substrate (pin 13) is internally separated from the negative supply (pin 14). They must be externally connected together.
- The switching transistor saturation voltage can be monitored at pin 4. To achieve this, a high voltage diode must be connected between the collector of the switching transistor and pin 4. Also a resistor must be connected from pin 4 to V^{+}_{CC} (see application diagram). This arrangement is useful when the chosen value of base current is very low and as a consequence the saturation voltage will be high. In this event, when $V_{CE(sat)}$ increases above 2.5V, the base current is interrupted before the normal end of the period. Remark : the TEA2019 can also operate without this protection.

TYPICAL APPLICATION

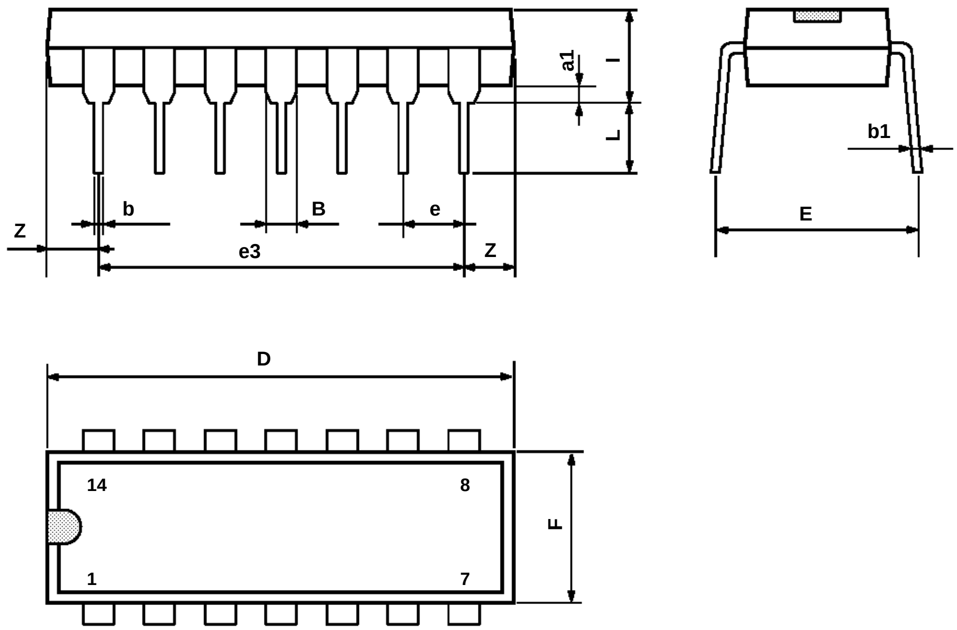


2019-08.EPS

- P_{MAX} = 60W
- Free-running Frequency : 15kHz
- $155V_{RMS} \leq V_{AC} \leq 250V_{RMS}$
- Outputs: 120V ± 3%, 0.4A
  24V ±3%, 0.5A
- V_{CE} Monitoring

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP



PM-DIP14.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

DIP14.TBL